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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,777	01/11/2002	Marc Chason	CMO1533I(72804)	8364

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FITCH EVEN TABIN AND FLANNERY
120 SOUTH LA SALLE STREET
SUITE 1600
CHICAGO, IL 60603-3406

EXAMINER
DOLAN, JENNIFER M

ART UNIT	PAPER NUMBER
2813	6

DATE MAILED: 10/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,777	CHASON ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-28 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-28 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1-4, 14, 15, and 21-28 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application Publication No. 2002/0119600 to Pierce.

Regarding claim 1, Pierce discloses a method comprising: providing an interposer (figure 3) having at least one semiconductor die (100) attached to a first side thereof (figure 3; paragraph 0030); and prior to placing the interposer on a printed wiring board, disposing an underfill (410) material on at least a portion of a second side thereof (figure 4; paragraph 0035).

Regarding claim 2, Pierce discloses providing an interposer having at least one interface electrode (400) disposed on a second side thereof (figure 4).

Regarding claim 3, Pierce discloses that the interface electrode comprises a solder bump (paragraph 0035, lines 1-2) disposed on a second side thereof (figure 4).

Regarding claim 4, Pierce discloses a step of adding at least one interface electrode to the second side of the interposer (figures 3 and 4; paragraph 0035).

Regarding claim 14, Pierce discloses providing a plurality of interposers disposed substantially co-planar to one another, wherein at least some of the interposers each have at least one semiconductor die (120) attached to one side thereof (figures 1 and 2; paragraph 22).

Regarding claim 15, Pierce discloses providing a plurality of singulated interposers (through dicing, in paragraphs 0034 and 0035).

Regarding claim 21, Pierce discloses a method comprising; providing a printed wiring board (paragraph 0035, lines 5 – 6 and 10-12); providing at least one interposer (figure 3) having a first side (bottom in figure 4) having at least one semiconductor die (100) affixed thereto; a second side (top in figure 4) having: an underfilling material (410) disposed thereon; and at least one interface electrode (400) at least partially exposed through the underfilling material (figure 4); and disposing the at least one interposer on the printed wiring board (paragraph 0035, lines 5 – 6 and 10-12).

Regarding claim 22, Pierce discloses that the interface electrode comprises a solder bump (paragraph 0035, lines 1 – 2).

Regarding claim 23, Pierce discloses further processing the interposer on the printed wiring board to at least partially harden the underfilling material (paragraph 0035, lines 4 – 12).

Regarding claim 24, it is implicit in Pierce that the processing includes heating the underfill material, because Pierce teaches that the underfill is solid at room temperature (paragraph 0035, lines 4 – 5), but the underfill will flow as a liquid at the same temperature as the solder flows, in order to promote adhesion (paragraph 0035, lines 5 – 8), which implies that the underfill is heated.

Regarding claim 25, Pierce discloses a device comprising: a pre-placement interposer (figure 3) having a first side (bottom in figure 4) having at least one semiconductor die (100) affixed thereto; and a second side (top in figure 4) having: an underfilling material (410) disposed thereon (figure 4); and at least one interface electrode (400) at least partially exposed through the underfilling material (figure 4).

Regarding claim 26, Pierce discloses that the interposer comprises means for physically (figure 4; paragraph 0035) and electrically (figure 4; paragraph 0032) coupling a semiconductor die to a printed wiring board.

Regarding claim 27, Pierce discloses that the underfilling material comprises adherence means for physically coupling the interposer to a printed wiring board (paragraph 0035, lines 4 – 9).

Regarding claim 28, Pierce discloses that the second side has a plurality of interface electrodes (400; figure 4) at least partially exposed through the underfilling material (figure 4).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5-13, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pierce in view of U.S. Patent No 6,335,571 to Capote et al (cited by applicant).

Regarding claim 5, Pierce fails to disclose adding at least one interface electrode to the second side after disposing the underfill.

Capote discloses a method of flip chip bonding in which interface electrodes (30) are added to the second side after disposing the underfill (column 5, lines 39-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the bonding method of Pierce so that the electrodes are added after disposing the underfill, as taught by Capote. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide the electrodes after disposing the underfill, because it leads to simpler and cheaper manufacturing of the solder bumps (Capote, column 6, lines 19-29), and additionally provides greater protection for the electrodes, by having a more uniform encapsulant, and allowing for the protection against oxidation of the electrodes, by providing fluxing agents before disposing the electrodes (column 4, lines 38-48; column 8, lines 39-60).

Regarding claim 6, Pierce fails to disclose disposing an underfill material on at least a portion of the second side thereof while simultaneously providing at least one aperture in the underfill material.

Capote discloses disposing an underfill material on at least a portion of the second side while simultaneously providing at least one aperture in the underfill material (column 11, lines 18-21).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Pierce by disposing an underfill while simultaneously providing at least one aperture in the underfill, as taught by Capote. The rationale is as follows:

One of ordinary skill in the art at the time the invention was made would have been motivated to provide apertures while disposing the underfill, because it is an art recognized equivalent procedure as disposing the underfill, and then forming apertures (Capote, column 11, lines 15 – 21), and thus the two procedures can be used interchangeably for disposing an underfill with apertures.

Regarding claim 7, Pierce fails to disclose adding at least one interface electrode in the at least one aperture.

Capote discloses adding interface electrodes in the apertures (column 11, lines 20-21).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Pierce as modified by Capote by adding interface electrodes in the apertures, as taught by Capote. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide interface electrodes in the apertures, because doing so allows the contact pads of the chip or interposer to be connected to the electrodes of a substrate or printed wiring board (Capote, column 11, lines 15 - 25), without requiring any complex or labor-intensive steps, and it allows for the cheap creation of solder bumps on a chip by simply filling in the apertures with molten solder (Capote, column 6, lines 19-29).

Regarding claim 8, Pierce fails to disclose forming an aperture in the underfill material and adding at least one interface electrode in the at least one aperture.

Capote discloses forming an aperture in the underfill material (column 5, lines 46 - 48) and adding at least one interface electrode in the at least one aperture (column 5, line 49).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Pierce such that apertures are formed in the underfill, and electrodes are added in the apertures, as taught by Capote. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide apertures and electrodes as taught by Capote, because doing so allows for the cheap and simple creation of solder bump electrodes on a chip by simply filling in the apertures with molten solder (Capote, column 6, lines 19-29). Additionally, providing apertures in the underfill, and then forming the electrodes allows the electrodes to be protected against oxidation from the moment they're added to the chip, due to the fluxing agents in the underfill (Capote, column 4, lines 38-48; column 8, lines 39-60).

Regarding claim 9, Pierce fails to disclose that disposing an underfill includes disposing a plurality of material layers.

Capote discloses disposing an underfill including a plurality of material layers (column 4, lines 18 - 29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the underfill deposition of Pierce such that a plurality of layers is deposited, as taught by Capote. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide a plurality of underfill layers, so that one layer can effectively compensate for thermal expansion and stress mismatches between the interposer and wiring board, while the other layer provides the flux adhesive properties necessary for oxidation and corrosion resistance of the electrodes, as well as for high adhesive strength

between the interposer and wiring board (Capote, column 4, lines 18-29 and 38-49 column 7, lines 57 - 67).

Regarding claim 10, Pierce fails to disclose exposing at least one of the layers to low-temperature processing.

Capote discloses exposing at least one of the layers to low-temperature processing (column 5, line 57).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Pierce so that at least one layer is exposed to low-temperature processing, as taught by Capote. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to expose at least one layer to low-temperature processing, because the underfill layers need to be cured, in order to promote hardness, durability, and solidity of the encapsulants, but the layers must be cured or processed at temperatures lower than the solder reflowing temperature, so that the solder bumps remain intact.

Regarding claim 11, Pierce fails to disclose exposing each material layer to low-temperature drying.

Capote discloses exposing each layer to low temperature curing (column 5, lines 42 – 44 and line 57), which inherently comprises an effect of drying the layers.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Pierce such that each layer is exposed to low temperature drying, as taught by Capote. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to expose the layers to low-temperature drying, because each underfill layer must be hardened and solidified, in order to promote

structural integrity of the encapsulant, as well as allow the formation of contact vias. This drying must occur at relatively low temperatures, so that the solder bumps remain intact, and don't liquefy or reflow (see Capote, column 5, lines 39 – 62).

Regarding claim 12, Pierce fails to disclose removing a portion of the underfill material to expose at least a portion of at least one interface electrode.

Capote discloses removing a portion of the underfill material to expose at least a portion of at least one interface electrode (column 9, lines 32 – 62).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Pierce such that a portion of the underfill is removed to expose the interface electrodes, as taught by Capote. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to apply the underfill, and then remove a portion of it to expose the electrodes, because the method eliminates the need for stencil printing, lithography, or temporary coatings, which decreases the complexity of the fabrication (Capote, column 9, lines 32 – 62).

Regarding claim 13, Pierce fails to disclose using chemical mechanical polishing, abrading, grinding, mechanical polishing, or laser ablation to expose a portion of the interface electrode.

Capote discloses using grinding or abrasion to expose the electrode (column 9, lines 59 – 62).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the procedure of Pierce as modified by Capote, such that abrading or grinding are used to remove portions of the underfill, as taught by Capote. The rationale is as

follows: One of ordinary skill in the art at the time the invention was made would have been motivated to use grinding or abrading, because the techniques are simple and viable means, from the standpoint of fabrication complexity and cost, for coarsely thinning the underfill, such that the electrodes are exposed.

Regarding claim 17, Pierce discloses disposing an underfill on the second side of a single interposer, but fails to disclose disposing an underfill on the second side of a plurality of interposers.

Capote discloses that the processing procedure, which includes the step of disposing the underfill, is performed on many chips simultaneously (column 11, lines 33- 41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Pierce so that the underfill is disposed on a plurality of interposers, as taught by Capote. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to dispose the underfill on a plurality of interposers, because it is time consumptive to repeat each processing step, including the deposition, electrode formation, and any alignments on each device separately, rather than performing the step once for an entire wafer, and disposing the underfill on a plurality of interposers decreases the fabrication time significantly.

Regarding claim 18, Pierce fails to disclose singulating the interposers after disposing the underfill material.

Capote discloses singulating the interposers after disposing the underfill (column 11, lines 33 – 41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the procedure of Pierce so that the interposers are singulated after disposing the underfill, as taught by Capote. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to singulate the interposers after disposing the underfill, so that the application of the underfill and solder bumps is done on many interposers simultaneously, thus decreasing processing time per device.

5. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pierce in view of U.S. Patent No. 6,323,062 to Gilleo et al. (cited by applicant).

Pierce discloses providing a wafer comprised of a plurality of interposers, but fails to disclose a panel comprised of a plurality of interposers.

Gilleo discloses a panel comprised of a plurality of flip chip components (figures 1 – 5; column 3, line 57 – column 4, line 10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the procedure of Pierce, so that the plurality of interposers are provided on a panel, as taught by Gilleo. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide a plurality of interposers on a panel, because Gilleo shows that in flip chip technology, it is advantageous to singulate the devices before applying the underfill, in order to eliminate the problems of cutting through hardened underfill material when singulating the devices (Capote, column 3, lines 45 – 57), while still allowing the underfill to be applied to each device in a single processing step.

6. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pierce in view of Capote as applied to claim 18 above, and further in view of U.S. Patent No 5,251,266 to Spigarelli et al.

Regarding claim 19, Pierce fails to disclose placing singulated interposers into a carrier to facilitate subsequent placement of the singulated interposers on a printed wiring board.

Spigarelli discloses placing singulated IC devices in a carrier (column 4, lines 1-4) to facilitate subsequent placement of the singulated devices on a printed wiring board (column 8, lines 38-45; column 13, lines 37-68).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Pierce as modified by Capote, such that singulated interposers are placed into a carrier, as taught by Spigarelli. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to place the singulated interposers into a carrier, so that the carrier features can be utilized to determine the position of each interposer, and thus allow for greater accuracy of placement onto a printed wiring board (Spigarelli, column 13, lines 37-68).

Regarding claim 20, Pierce fails to disclose placing at least some of the singulated interposers into at least one of a tape and reel carrier, a waffle pack, and a matrix tray.

Spigarelli discloses placing IC devices into a matrix tray (column 4, lines 1-4; column 8, lines 38-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Pierce as modified by Capote, such that the singulated interposers are placed in a matrix tray, as taught by Pierce. The rationale is as follows: One of

ordinary skill in the art at the time the invention was made would have been motivated to place the interposers in a matrix tray, so that the position of each interposer is a known parameter, thus enabling automated pick and place bonding to a printed wiring board (Spigarelli, column 8, lines 38-45; column 13, lines 37-68).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,399,178 to Chung discloses flip chip components with a pre-form underfill applied to the component before mounting on a printed wiring board.

U.S. Patent No. 6,281,046 to Lam discloses a package wherein an underfill flux material is applied to a substrate before an interposer is attached to the substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (703) 305-3233. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (703) 305-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd
October 23, 2002

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800